501.37426CX1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	I. FUJII et al
Serial No.:	09/928,497
Filed:	August 14, 2001
For:	SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
Group:	2827
Examiner:	L. Cruz

#5
9/24/02
Jm.

RESPONSE TO FIRST OFFICE ACTION PURSUANT TO 37 CFR §1.111

Assistant Commissioner Of Patents
Washington, D. C. 20231

Sept. 18, 2002

Sir:

In reply to the outstanding Office Action, dated June 18, 2002, the following responsive remarks are respectfully submitted, in connection with the above-identified application.

Reconsideration as well as favorable action therefor of the above-referenced application in consideration of the supportive discussion and arguments presented hereinbelow is respectfully requested.

An objection was made to the drawings for the reason that, allegedly, reference numeral 13 in Fig. 11 of the drawings is "not mentioned in the description." A review of the specification of the present application clearly shows that reference number "13" is described in the sentence beginning in the last line of page 32, wherein it is stated " ... select signal YS is set from a YS driver 53 in a

column decoder circuit 13....**[emphasis added]**". Since this objection to the drawings was shown to be clearly improper, it is accordingly being traversed. Therefore, reconsideration and withdrawal of the same is respectfully requested.

The additional objection to the drawings, as detailed on page 2 of the outstanding Office Action, regarding the missing reference symbol "VPP-C," which is mentioned on page 6, line 2, of the present specification, is noted. A careful review was made regarding this matter and, it was discovered that a minor drafting error occurred with regard to the insertion of reference characters when the drawings were being prepared. Specifically, in Fig. 1 of the drawings, it is noted that the reference symbol "VPP-G" was inadvertently inserted in two adjacent locations. It was intended for the second labeled block from the top to be labeled instead as the "VPP-C" block, consistent with that referred to on page 6, lines 2-3, of the present specification. As is clearly seen from the related description in the paragraph bridging pages 5-6 of the present specification, the dynamic RAM, amongst other components thereof, does include a boosted voltage generator (VPP-G) and also a control circuit (VPP-C) for controlling the operation of the boosted voltage generator (VPP-G). Consistent with this, therefore, the second block which was incorrectly labeled as VPP-G in Fig. 1 of the drawings, is being appropriately re-labeled as that originally intended, namely, to read as VPP-C. Accordingly, in consideration of the Examiner's requirement to submit a "proposed drawing correction or corrected drawings," at the present time, applicants are submitting herewith a paper entitled, "Request for Approval to Amend the Drawings" concerning the re-labeling of the lower internal block labeled as "VPP-G" to the correct symbol VPP-C. Since the accompanying drawing amendment proposal is being submitted to remove a minor informality, acceptance and formal entry therefor

of the same is respectfully requested. With acceptance of this drawing proposal, a formal correction thereof will be effected in connection with the submission of corrected formal drawings at such appropriate time as subsequently to applicants receiving an official Notification of Allowability of the above-identified application.

According to the outstanding Office Action, also, claims 1-3 were rejected under 35 USC §102(e) as anticipated by Hidaka (US 5,880,493). It will be shown, hereinbelow, the invention according to claims 1-3 was not taught by Hidaka.

In Hidaka's Fig. 13 layout/interconnection scheme, the Examiner considers lines Lc2, Lb1 and FT7 as the "first interconnection (Lc2)," the "second interconnection (Lb1)" and the "third interconnection (FT7)", respectively. It should be noted, however, independent claims 1 and 2 make reference to a first line, a second line as well as to a "third line" and not to first through third interconnections, as is noted in the rejection. Nonetheless, even if the expressions "first line," "second line" and "third line", according to claims 1 and 2, were to be read instead as first, second and third interconnections, as is argued in the rejection, Hidaka still failed to teach the present invention. For example, according to claims 1 and 2, the present invention calls for the "third line" to effect a connection between the second line and the terminal of the MOSFET in the unit area (e.g., CC2). This, of course, necessitates a connection of the "third line" with the "second line". This is also featured with regard to claim 2, in which the invention calls for the "third line" to connect the "second line" and a "terminal of said circuit" (in the unit area). However, with regard to Hidaka's Fig. 13 layout interconnection scheme, it is noted that the third line (or interconnection (FT7)) is <u>not</u> connected to the second line or (second interconnection (Lb1)), which is in clear contradistinction with that which would be necessitated by the present claimed subject matter. For line Lb1 to be connected to

a MOSFET or circuit within, for example, unit area CC2 or CC1, there must necessarily be a connection between the third line (FT7) and the second line (Lb1). Such, however, is not disclosed by Hidaka, referring to Hidaka's Fig. 13 arrangement which was cited in the rejection. It is submitted, therefore, the invention according to claims 1 and 2 and therefor also according to claim 3 (dependent on claim 2) is clearly defining thereover.

Claims 1-3 were additionally rejected under 35 USC §103 as "claiming the same invention as that of claims 1-18 of prior, U.S. patent number 6,274,895." It will also be shown, hereinbelow, that the invention according to claims 1 and 3 is substantially different than the claimed disclosure of the above-named prior, U.S. patent. Specifically, the recited limitation "wherein said third line is separated from said first line electrically," found in each of independent claims 1 and 2 of the present application, is not disclosed in connection with claims 1-18 of the above-named prior, U.S. patent (henceforth referred to as Fujii P1). Claims 17 and 18, which appear to have the closest wording to that of the present claimed subject matter call for a semiconductor integrated circuit device including unit areas, first through third lines and wiring areas, similarly as that presently called for, although in a somewhat modified form therefrom. However, the featured aspect of the third line being electrically separated from that of the first line is not disclosed in the claims of Fujii P1 in the manner as that presently recited.

Substantive differences are also present between claims 1-3 of the present application with that of the disclosed subject matter in connection with claims 1-16 in Fujii P1. For example, while the present invention calls for first through third lines, the disclosed subject matter according to claims 1, etc., in Fujii P1, calls for first through third interconnections. The disclosure according to claim 1 links the

referred-to "one or plural MOSFETs" to a "specific logical function," which is not specifically called for in claims 1-3 of the present application. Moreover, the disclosed subject matter in connection with the last two "wherein" clauses of claim 1 are also not specifically called for in the present claims. Additional differences including differences that are substantive in nature also exist between the claimed disclosure in Fujii P1 and that according to claims 1-3 of the present application.

It is clearly apparent therefore that the present claims are not specifically directed to the same invention as that of the claim disclosure in Fujii P1.

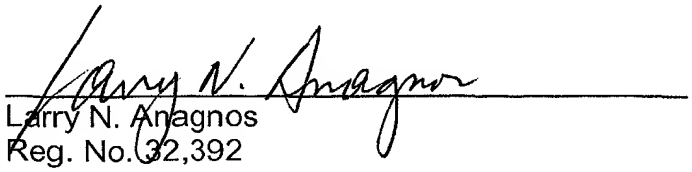
For a statutory double-patenting rejection, namely, a rejection under 35 USC §101, to be proper, the question to be determined is whether or not the same invention is being claimed twice. The "same" invention means identical subject matter. If identical subject matter is being claimed, then it can be argued that the claims in the present application could be literally infringed without literally infringing the corresponding claim(s) in the patent. However, in view of the differences in scope between that of the present claims and the claims of Fujii P1, as was shown hereinabove, the standard for satisfying the criteria of a statutory double-patenting rejection, it is submitted, has not been met. Therefore, this rejection is accordingly traversed and withdrawal of the same is respectfully requested.

Therefore, in view of the supportive discussion and arguments presented hereinabove, reconsideration and withdrawal of all outstanding objections/rejections, as well as a favorable action therefor on pending claims 1-3 and an early formal Notification of Allowability of the above-identified application is respectfully requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the

filing of this paper, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (501.37426CX1), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP



Larry N. Anagnos
Reg. No. 32,392

LNA/dks
703-312-6600